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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/862,941	05/22/2001	Mark Flood	01AB077	9740

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EXAMINER

SHIN, KYUNG H

ART UNIT	PAPER NUMBER
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2143

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/862,941

Applicant(s)

FLOOD ET AL.

Examiner

Kyung H. Shin

Art Unit

2143

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 January 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-52 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-52 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. This action is responding to application papers dated 1/6/2005
2. Claims **1-52** are pending. Claim 1 has been amended. Independent claims are **1, 38, 39 and 52**.

Response to Arguments

3. Applicant's arguments filed 1/6/2005 have been fully considered but they are not persuasive.

- 3.1 Applicant argues that the referenced prior art does not disclose "*... an apparatus ... for time synchronization ...*". (see Remarks Page 10, Lines 20-21) An apparatus is defined as "*... an integrated group of devices used for a particular purpose ...*". Voth (6,199,169) discloses a system (i.e. an apparatus) capable of performing a particular single purpose, which is time synchronization. The time synchronization apparatus interfaces with the interconnected system to perform synchronization functions. (see Voth col. 2, lines 51-54: apparatus for time synchronization ; col. 2, lines 57-58: interfaces with other host processors)

- 3.2 Applicant argues that the referenced prior art does not disclose network data transmissions consisting of “ ... *data used for purposes other than absolute time synchronization* ... ”. (see Remarks page 12, lines 3-4) Voth in view of Kuribayashi (6,775,246) discloses the capability to transmit time synchronization information and non time synchronization data over an interconnected network. (see Kuribayashi col. 8, lines 29-34; col. 9, lines 2-4: clock signals (i.e. time synchronization information) and transmitting and receiving data (i.e. non time synchronization data))

Claim Rejections 35 USC § 102

4. The following is a quotation of appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1-7, 13-28, 30-34, 38-46, 48-52**, are rejected under 35 U.S.C. 102(e) as being unpatentable over **Voth** (US Patent No. 6,199,169: System and method for synchronizing time across a computer cluster, Filed Dec. 15, 1998).

Regarding Claim 1, Voth discloses a time synchronization apparatus for synchronizing

operation of a first controller with that of a second controller in a control system, the synchronization apparatus comprising:

a processor interface for interfacing the synchronization apparatus with a host processor; (see col. 4, lines 17-27)

a transmitter adapted to transmit synchronization information and data to a network in the control system; (see col. 2, lines 57-60)

a receiver adapted to receive synchronization information and data from the network; (see col. 2, lines 60-61) and

a timing system with a clock that maintains an indication of time according to information received from one of the network and the host processor. (see col. 2, lines 51-54)

Regarding Claim 2, Voth discloses the time synchronization apparatus of claim 1, being configurable to operate as one of a synchronization master and a synchronization slave. (see col. 4, lines 35-42)

Regarding Claims 3, 20, Voth discloses the time synchronization apparatus of claim 1, 14, being configured to operate as a synchronization master, wherein the transmitter periodically transmits message frames at a fixed period. (see col. 4, lines 43-47)

Regarding Claims 4, 15, Voth discloses the time synchronization apparatus of claim 3,

Art Unit: 2143

14, wherein the fixed period is about 50 μ s. (According to Applicant's specification on page 28 at lines 15-16, it states, "...the synchronization component can transmit (broadcast) a frame every 50 μ s or some other fixed time period." see Voth col. 4, lines 43-54; where the reference states that the update period is performed at a regular or periodic fixed time period which can be equal to 50us or some other time period.)

Regarding Claims 5, 16, Voth discloses the time synchronization apparatus of claim 3, 14, wherein the transmitter transmits a message frame having an LCM indicator at a least common multiple (LCM) interval. (see Voth col. 4, lines 43-54: "...use a repeating update cycle...Update cycle...includes an initial calculation ... scheduling period...a time adjustment period." Applicant's specification states on page 13 at lines 20-26 that "...least common multiple (LCM) period, ...can be set to the lowest integer multiple of periodic tasks..." (i.e. set to 1) Thus, LCM is tied to reference's periodic update cycle.)

Regarding Claims 6, 17, Voth discloses the time synchronization apparatus of claim 5, 16, wherein the LCM interval is 600ms. (see Voth col. 4, lines 43-54: "...use a repeating update cycle...Update cycle...includes an initial calculation...scheduling period...a time adjustment period." Applicant's specification status on page 13 at lines 20-26 that "...600ms is exemplary... other LCM periods fall within the scope of the present invention..." Thus, LCM is equal to periodic update cycle.)

Regarding Claims 7, 30, Voth discloses the time synchronization apparatus of claim 3,

Art Unit: 2143

14, being configured as a synchronization master, wherein the transmitter transmits message frames having multiplexed data and direct data. (see col. 3, lines 1-9)

Regarding Claim 13, Voth discloses the time synchronization apparatus of claim 7, wherein the timing system is adjustable according to information received from the host processor. (see col. 2, lines 51-54)

Regarding Claim 14, Voth discloses the time synchronization apparatus of claim 1, being configured as a synchronization slave, wherein the receiver receives message frames at a fixed period, and wherein the timing system is adjusted according to the fixed period. (see col. 4, lines 43-47)

Regarding Claim 18, Voth discloses the time synchronization apparatus of claim 16, wherein the timing system is adjusted according to the LCM indicator. (see col. 4, lines 47-44)

Regarding Claim 19, Voth discloses the time synchronization apparatus of claim 16, wherein the receiver interrupts the host processor according to the LCM indicator. (see col. 4, lines 43-47)

Regarding Claim 21, Voth discloses the time synchronization apparatus of claim 20,

Art Unit: 2143

wherein the message frames received and transmitted by the receiver and transmitter, respectively, comprise multiplexed data and direct data. (see col. 5, lines 18-25)

Regarding Claims 22, 43, Voth discloses the time synchronization apparatus of claim 21, 39, wherein the data field comprises 6 32 bit words, and wherein the amount of multiplexed data and the amount of direct data in each message frame is configurable. (see col. 5, lines 50-59; col. 6, lines 10-14: *"Different implementations of the present invention may use difference sizes for an, or all, of these components."*, where reference states that different sizes and values (i.e. amounts of data: 32 bit words) can be used for the data contained within message frames and therefore is configured by implementation.)

Regarding Claim 23, Voth discloses the time synchronization apparatus of claim 22, wherein each message frame comprises a direct data portion and a multiplexed data portion, wherein the direct data comprises the direct data portion of a single frame, and wherein the multiplexed data comprises the multiplexed data portions of a plurality of frames. (see col. 5, lines 18-25)

Regarding Claim 24, Voth discloses the time synchronization apparatus of claim 23, wherein the multiplexed data portion comprises configuration information indicative of the amount of multiplexed data and the amount of direct data in each message frame. (see col. 5, lines 26-29; col. 5, lines 50-59)

Regarding Claims 25, 26, Voth discloses the time synchronization apparatus of claim 24, wherein the receiver presents direct data or multiplexed data from received message frames to the host processor at the fixed or a multiple of the fixed period. (see col. 4, line 67 - col. 5, line 5)

Regarding Claim 27, Voth discloses the time synchronization apparatus of claim 14, comprising a multiplier receiving an operand from the receiver, a multiplication value on the host processor, and providing a multiplication result value to at least one of the host processor and the transmitter, wherein the multiplication result value is the product of the multiplication value and the operand. (see col. 5, lines 18-20)

Regarding Claims 28, 32, Voth discloses the time synchronization apparatus of claim 27, 30, wherein the direct data received in the message frame comprises the operand. (see col. 5, lines 18-25)

Regarding Claim 31, Voth discloses the time synchronization apparatus of claim 30, wherein at least a portion of the direct data in the message frames transmitted by the transmitter is provided to the transmitter by the receiver, wherein the direct data from a received message frame is passed through to the transmitter. (see col. 6, lines 31-37)

Regarding Claims 33, 34, Voth discloses the time synchronization apparatus of claim

30, wherein at least a portion of the direct data and multiplexed data in the message frames transmitted by the transmitter is provided to the transmitter by the host processor. (see col. 5, lines 20-25)

Regarding Claim 38, Voth discloses a synchronization module in a control chassis for synchronizing operation of a first controller in the control chassis with that of a second controller outside the control chassis, comprising:

a host processor in communication with the first controller via a backplane bus in the control chassis; (see col. 4, lines 17-27)

a transmitter adapted to transmit synchronization information and data to a network in the control system; (see col. 2, lines 57-60)

a receiver adapted to receive synchronization information and data from the network; (see col. 2, lines 60-61)

a timing system with a clock and maintaining an indication of time according to information received from one of the network and the host processor; (see col. 2, lines 51-54) and

a synchronization circuit operatively associated with the host processor, the transmitter, the receiver, and the timing system, and configurable by the host processor to operate the module as one of a synchronization master and a synchronization slave. (see col. 4, lines 35-42)

Regarding Claim 39, Voth discloses a synchronization circuit for synchronizing

Art Unit: 2143

operation of a first controller with that of a second controller in a control system, comprising:

a processor interface for interfacing the synchronization circuit with a host processor; (see col. 4, lines 17-27)

a transmitter component adapted to transmit synchronization information and data to a network in the control system; (see col. 2, lines 57-60)

a receiver component adapted to receive synchronization information and data from the network; (see col. 2, lines 60-61) and

a timing system with a clock and maintaining an indication of time according to information received from one of the network and the host processor, wherein the synchronization circuit is configurable by the host processor to operate as one of a synchronization master and a synchronization slave. (see col. 2, lines 51-54)

Regarding Claims 40, 41, Voth discloses the system of claim 39, wherein the transmitter component periodically transmits message frames comprising direct data, and wherein the direct data is obtained from at least one of the receiver, the host processor, and the multiplier. (see col. 5, lines 18-25)

Regarding Claim 42, Voth discloses the system of claim 39, wherein the transmitter component periodically transmits message frames comprising multiplexed data, and

Art Unit: 2143

wherein the multiplexed data is obtained from the host processor. (see col. 4, lines 43-47)

Regarding Claim 44, Voth discloses the system of claim 39, wherein the receiver component periodically receives message frames comprising direct data, multiplexed data, and status information from the network, and wherein the synchronization circuit provides at least one of received direct data, received multiplexed data and received status information from the receiver component to the host processor. (see col. 6, lines 31-37)

Regarding Claim 45, Voth discloses the system of claim 44, further comprising a multiplier operating on the received direct data, and wherein the synchronization circuit provides a multiplier result value from the multiplier to the host processor. (see col. 5, lines 18-20)

Regarding Claim 46, Voth discloses the system of claim 45, wherein the synchronization circuit provides a multiplication value to the multiplier from the host processor. (see col. 5, lines 18-20)

Regarding Claim 48, Voth discloses the system of claim 39, wherein the transmitter component periodically transmits message frames comprising direct data, multiplexed data, and configuration information, and wherein the synchronization circuit provides at

least one of the direct data, multiplexed data, and configuration information to the transmitter component from the host processor. (see col. 5, lines 18-25)

Regarding Claim 49, Voth discloses the system of claim 39, wherein the transmitter component periodically transmits message frames having synchronization information, wherein the synchronization information is obtained from the timing system, and wherein the timing system is adjusted according to at least one of synchronization information received from the network and synchronization information from the host processor. (see col. 4, lines 43-47; col. 2, lines 51-54)

Regarding Claim 50, Voth discloses the system of claim 39, wherein the synchronization circuit interrupts the host processor according to receipt of an LCM indicator by the receiver. (see col. 4, lines 43-47)

Regarding Claim 51, Voth discloses the system of claim 39, wherein the synchronization circuit interrupts the host processor periodically for presentation of at least one of direct data and multiplexed data from the receiver to the host processor. (see col. 4, lines 43-47)

Regarding Claim 52, Voth discloses a synchronization system for synchronizing a first controller with a second controller in a control system, comprising:
means for interfacing the synchronization circuit with a host processor; (see col. 4, lines

Art Unit: 2143

17-27)

means for transmitting synchronization information and data to a network in the control system; (see col. 2, lines 57-60)

means for receiving synchronization information and data from the network; (see col. 2, lines 60-61) and

means for maintaining an indication of time according to information received from one of the network and the host processor, wherein the synchronization circuit is configurable by the host processor to operate as one of a synchronization master and a synchronization slave. (see col. 2, lines 51-54)

Claim Rejection 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. **Claims 8, 9, 10, 11, 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Voth et al. (US Patent No. 6,199,169) in view of **Ramussen et al.** (US Patent No. 6,449,732: Method and apparatus for processing control using a multiple redundant processor control system).

Art Unit: 2143

Regarding Claim 8, Voth discloses a header with flag bytes, a control byte and a data field and a bitmask used in error detection for data within the message frames. Voth does not disclose specifically the CRC technique in error detection procedures. However, Rasmussen discloses the time synchronization apparatus of claim 7, wherein the same comprises three flag bytes, a control byte, a data field comprising the multiplexed data and the direct data, and two CRC bytes. (see Rasmussen col. 14, lines 1-4: *"Calculates and check the received CRCs..."* ; col. 14, lines 16-19: *"Calculates and send the transmit CRCs..."*)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Voth with the error detection capabilities as taught by Rasmussen. One of ordinary skill in the art would be motivated to modify Voth to employ the invention of Rasmussen in order to enhance the processing of time synchronization information with an extension in error detection capabilities. (see Rasmussen col. 5, lines 24-27: *"...hardware loop-back fault detection, CRC checking...."*)

Regarding Claims 9, 12, Voth discloses the time synchronization apparatus of claim 8, wherein the data field comprises 6 32 bit words, and wherein the amount of multiplexed data and the amount of direct data in each message frame is configurable. (see col. 5, lines 50-59; col. 6, lines 10-14: *"Different implementations of the present invention may use difference sizes for an, or all, of these components."*, where reference states that

Art Unit: 2143

different sizes and values (i.e. amounts of data: 32 bit words) can be used for the data contained within message frames and therefore is configured by implementation.)

Regarding Claim 10, Voth discloses the time synchronization apparatus of claim 9, wherein each message frame comprises a direct data portion and a multiplexed data portion, wherein the direct data comprises the direct data portion of a single frame, and wherein the multiplexed data comprises the multiplexed data portions of a plurality of frames. (see col. 5, lines 18-25)

Regarding Claim 11, Voth discloses the time synchronization apparatus of claim 10, wherein the multiplexed data portion comprises configuration information indicative of the amount of multiplexed data and the amount of direct data in each message frame. (see col. 5, lines 26-32; col. 5, lines 48-59)

8. **Claims 29, 35, 36, 37, 47** are rejected under 35 U.S.C. 103(a) as being unpatentable over Voth et al. (US Patent No. 6,199,169) in view of **Kuribayashi et al.** (US Patent No. 6,775,246: Method of determining master and slaves by communication capability of network nodes).

Voth discloses a time synchronization apparatus with designated master and slave nodes and a timing system with a periodic and continuously updating feature. (see Voth col. 35, lines 45: *"... a distributed system that maintains the synchronization between time clocks ..., one of the nodes...assumes a master role. The remaining*

Art Unit: 2143

nodes 102 then function as slaves ...To synchronize time clocks 212, master node 102a and slave nodes 102b-d use a repeating update cycle")

Regarding Claims 29, 47, Voth does not disclose an apparatus to process status information from an upstream device. However, Kuribayashi discloses the time synchronization apparatus of claim 14, 44, wherein the message frame comprises a status component indicative of the status of an upstream device and error counter, wherein the receiver provides the status component to the host processor. (see Kuribayashi col. 2, lines 9-19; col. 8, lines 37-42)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Voth with an apparatus to process status information from an upstream device as taught by Kuribayashi. One of ordinary skill in the art would be motivated to employ the invention of Kuribayashi in order to extend the processing of time synchronization information to control the operation of additional devices. (see Kuribayashi col. 1, lines 53-57: "...provide a novel communication control apparatus, which permits the proper and simple setting of transmission/reception nodes...synchronization information in a high-speed network.")

Regarding Claim 35, Voth does not disclose a procedure to process a status signal from an upstream device in a daisy-chain. However, Kuribayashi discloses the time synchronization apparatus of claim 1, being configured as an intermediate node in a daisy-chain topology, the receiver receiving synchronization information from an upstream device in the daisy-chain, and the transmitter transmitting the synchronization

Art Unit: 2143

information to at least one downstream device in the daisy-chain. (see Kuribayashi col. 2, lines 9-19; col. 8, lines 37-42)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Voth in order for an apparatus to process status information from an upstream device as taught by Kuribayashi. One of ordinary skill in the art would be motivated to employ the invention of Kuribayashi in order to extend the processing of time synchronization information controlling the operation of networked devices. (see Kuribayashi col. 1, lines 53-57: "...provide a novel communication control apparatus, which permits the proper and simple setting of transmission/reception nodes ...synchronization information in a high-speed network.")

Regarding Claim 36, Voth discloses the time synchronization apparatus of claim 35, wherein the receiver receives message frames at a fixed period, and wherein the transmitter transmits message frames at the fixed period comprising direct data and multiplexed data. (see col. 4, lines 47-54)

Regarding Claim 37, Voth discloses the time synchronization apparatus of claim 36, wherein at least a portion of the direct data in the message frames transmitted by the transmitter is provided to the transmitter by the receiver, wherein the direct data from a received message frame is passed through to the transmitter. (see col. 4, lines 47-54)

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kyung H Shin whose telephone number is 703-305-0711. The examiner can normally be reached on 9 am - 7 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David A Wiley can be reached on 703-308-5221. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2143

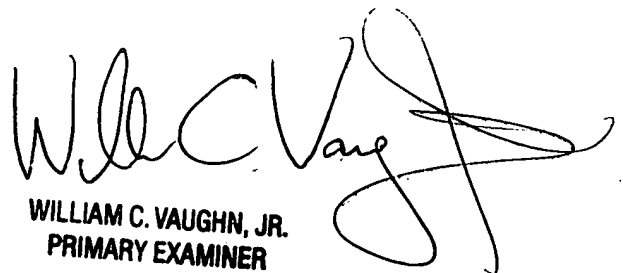
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KHS

Kyung H Shin
Patent Examiner
Art Unit 2143

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June 27, 2005



WILLIAM C. VAUGHN, JR.
PRIMARY EXAMINER